Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**BACK CONTACT IS ANODE**

**TOP CONTACTS ARE ANODE**

**Top Material: Au**

**Backside Material: Au**

**Bond Pad Size: .001” x .001” min.**

**Backside Potential: ANODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .016” X .016” DATE: 3/14/22**

**MFG: ADVANCED SEMI THICKNESS .006” P/N: ASTD1020**

**DG 10.1.2**

#### Rev B, 7/19/02